



1/3-Inch 1.2 Mp CMOS Digital Image Sensor with Global Shutter

AR0135AT Datasheet, Rev. 2

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Features

- ON Semiconductor's Next Generation Global Shutter Technology
- Superior low-light performance
- HD video (720p60)
- Video/Single Frame mode
- Flexible row-skip modes
- On-chip AE and statistics engine
- Parallel and serial output
- Support for external LED or flash
- Auto black level calibration
- Context switching

Applications

- Automotive scene processing
- Scanning and machine vision
- 720p60 video applications

General Description

The ON Semiconductor AR0135AT is a 1/3-inch 1.2Mp CMOS digital image sensor with an active-pixel array of 1280H x 960V. It is designed for low light performance and features a global shutter for accurate capture of moving scenes and synchronization with pulsed light sources. It includes sophisticated camera functions such as auto exposure control, windowing, scaling, row skip mode, and both video and single frame modes. It is programmable through a simple two-wire serial interface. The AR0135AT produces extraordinarily clear, sharp images, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including automotive scene processing.

Table 1: Key Parameters

Parameter	Typical Value
Optical format	1/3-inch (6 mm)
Active pixels	1280H x 960V = 1.2 Mp
Pixel size	3.75 μm
Color filter array	Monochrome
Shutter type	Global shutter
Input clock range	6 – 50 MHz
Output pixel clock (maximum)	74.25 MHz

Table 1: Key Parameters (continued)

Parameter	Typical Value	
Output	Serial	HiSPi
	Parallel	12-bit
Frame rate	Full resolution	54 fps
	720p	60 fps
Responsivity	Monochrome	3.22 V/lux*sec
		42 ke-/lux*sec
SNR _{MAX}		40.7 dB
Dynamic range		67.7 dB
Supply voltage	I/O	1.8 or 2.8 V
	Digital	1.8 V
	Analog	2.8 V
	HiSPi	0.4 V
Power consumption		<400 mW
Operating temperature		–40°C to + 105°C (ambient)
		–40°C to + 120°C (junction)
Package options		9 x 9 mm 64-pin iBGA
		Bare die



AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor Ordering Information

Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
AR0135AT2M00XUEA0-DPBR	Mono, iBGA	Dry Pack with Protective Film, Double Side BBAR Glass
AR0135AT2M00XUEA0-DRBR	Mono, iBGA	Dry Pack without Protective Film, Double Side BBAR Glass
AR0135AT2M00XUEA0-TPBR	Mono, iBGA	Tape & Reel with Protective Film, Double Side BBAR Glass
AR0135AT2M00XUEA0-TRBR	Mono, iBGA	Tape & Reel without Protective Film, Double Side BBAR Glass
AR0135AT2M00XUEAD3-GEVK	Mono, iBGA, Demo3 Kit	
AR0135AT2M00XUEAH3-GEVB	Mono, iBGA, Head Board	
AR0135AT2M00XPD20	Mono, Bare Die	



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General Description

The ON Semiconductor™ AR0135AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full-resolution image at 54 frames per second (fps). It outputs 12-bit raw data, using either the parallel or serial (HiSPi) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock. A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

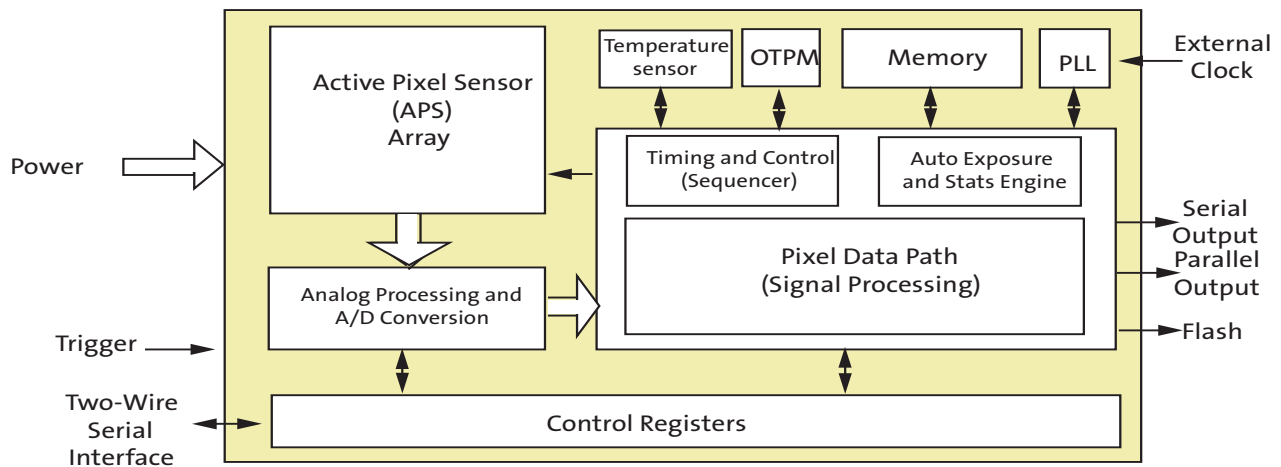
The AR0135AT includes additional features to allow application-specific tuning: windowing, adjustable auto-exposure control, auto black level correction, on-board temperature sensor, and row skip and digital binning modes.

The sensor is designed to operate in a wide temperature range (–40°C to +105°C).

Functional Overview

The AR0135AT is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 74.25 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor.

Figure 1: Block Diagram



User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.2 Mp Active-Pixel Sensor array. The AR0135AT features global shutter technology for accurate capture of moving images. The exposure of the entire array is controlled by programming the integration time by register setting. All rows simultaneously integrate light prior to readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital



AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor Features Overview

processing signal chain (which provides further data path corrections and applies digital gain). The pixel data are output at a rate of up to 74.25 Mp/s, in parallel to frame and line synchronization signals.

Features Overview

The AR0135AT Global Sensor shutter has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0135AT Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- **Operating Modes**
The AR0135AT works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes. Trigger mode is not compatible with the HiSPi interface.
- **Window Control**
Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital binning and skipping modes are supported, as are vertical and horizontal mirror operations.
- **Context Switching**
Context switching may be used to rapidly switch between two sets of register values. Refer to the AR0135AT Developer Guide for a complete set of context switchable registers.
- **Gain**
The AR0135AT Global Shutter sensor can be configured for analog gain of up to 8x, and digital gain of up to 8x.
- **Automatic Exposure Control**
The integrated automatic exposure control may be used to ensure optimal settings of exposure and gain are computed and updated every other frame. Refer to the AR0135AT Developer Guide for more details.
- **HiSPi**
The AR0135AT Global Shutter image sensor supports two or three lanes of Streaming-SP or Packetized-SP protocols of ON Semiconductor's High-Speed Serial Pixel Interface.
- **PLL**
An on chip PLL provides reference clock flexibility and supports spread spectrum sources for improved EMI performance.
- **Reset**
The AR0135AT may be reset by a register write, or by a dedicated input pin.
- **Output Enable**
The AR0135AT output pins may be tri-stated using a dedicated output enable pin.
- **Temperature Sensor**
The temperature sensor is only guaranteed to be functional when the AR0135AT is initially powered-up or is reset at temperatures at or above 0°C.
- **Black Level Correction**
- **Row Noise Correction**
- **Column Correction**
- **Test Patterns**
Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to grey, and a walking 1s test pattern.

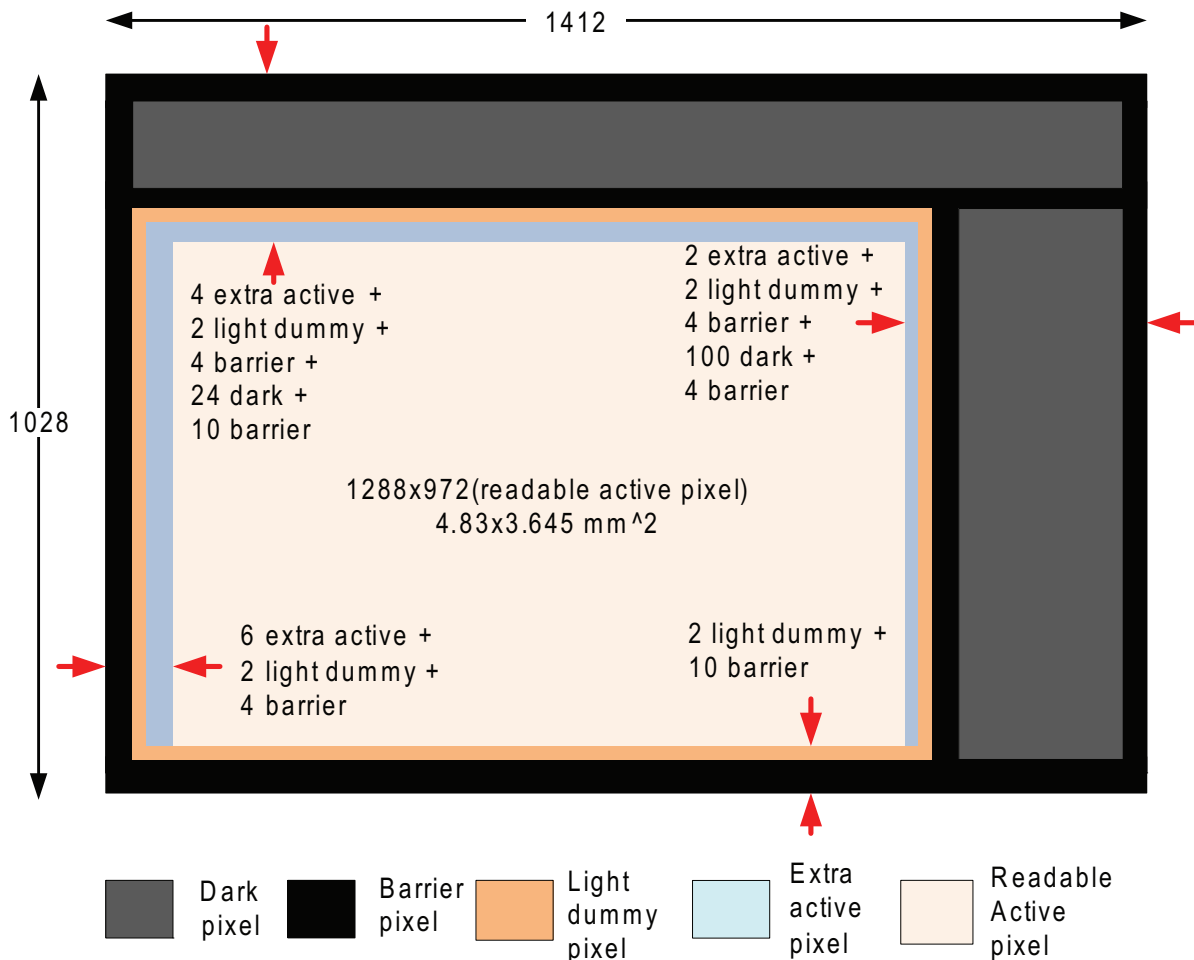


Pixel Data Format

Pixel Array Structure

The AR0135AT pixel array is configured as 1412 columns by 1028 rows, (see Figure 2). The dark pixels are optically black and are used internally to monitor black level. Of the right 108 columns, 64 are dark pixels used for row noise correction. Of the top 24 rows of pixels, 12 of the dark rows are used for black level correction. There are 1288 columns by 972 rows of optically active pixels that can be readable. While the sensor's format is 1280 x 960, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome version. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out. The optical center of the readable active pixels can be found between X_ADDR 643 and 644, and between Y_ADDR 485 and 486.

Figure 2: Pixel Array Description





Default Readout Order

By convention, the sensor core pixel array is shown with the first addressable (logical) pixel (0,0) in the top right corner. This reflects the actual layout of the array on the die. Also, the physical location of the first pixel data read out of the sensor in default condition is that of pixel (112, 44).

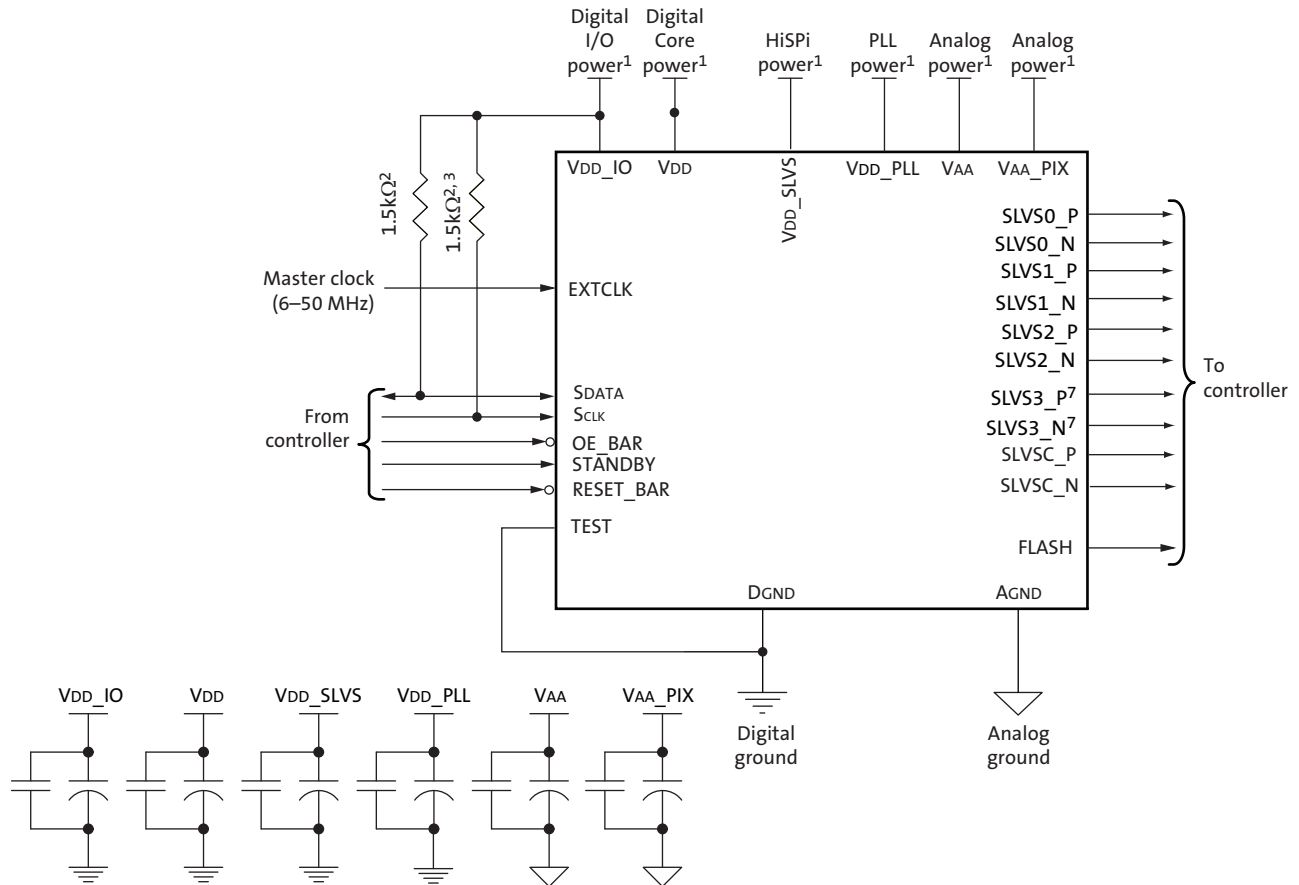


AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor Configuration and Pinout

Configuration and Pinout

The figures and tables below show a typical configuration for the AR0135AT image sensor and show the package pinouts.

Figure 3: Typical Configuration: Serial Four-Lane HiSPi Interface

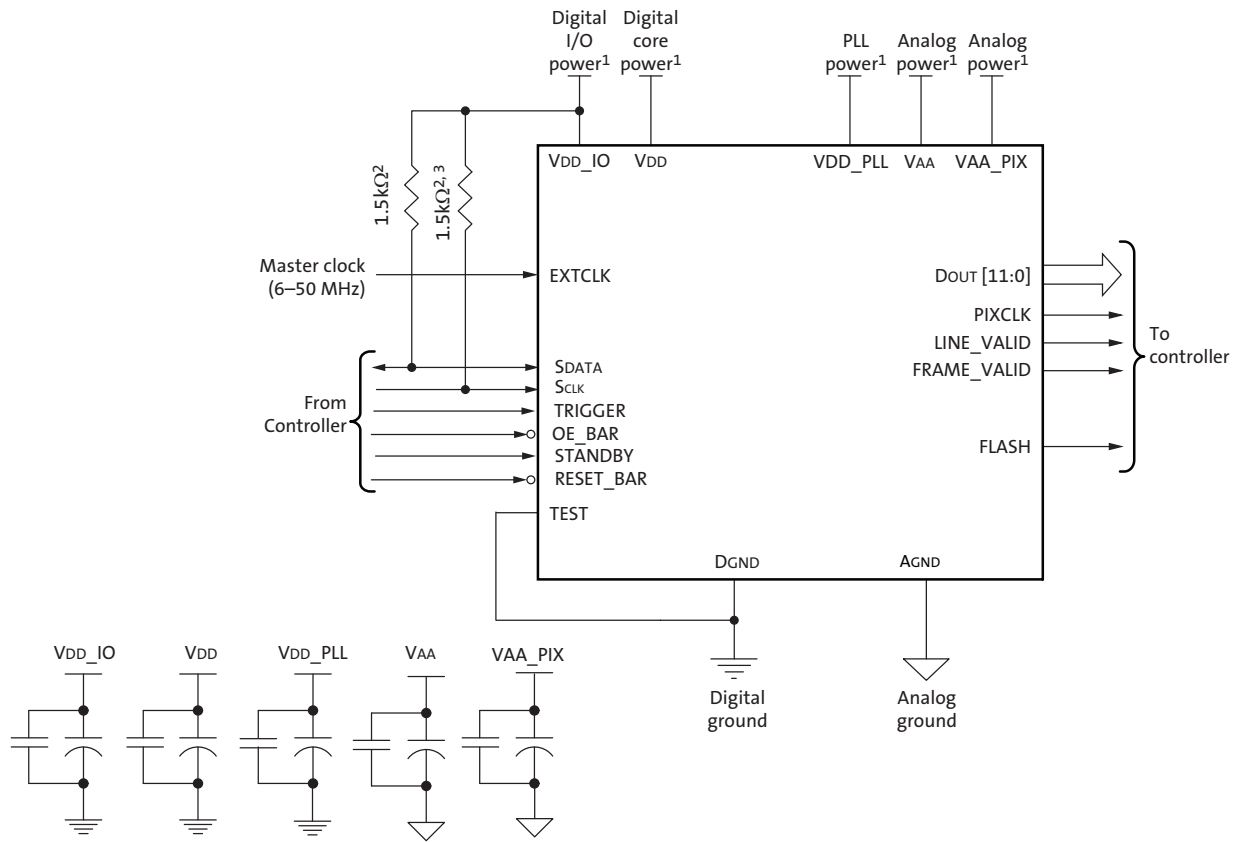


- Notes:
1. All power supplies must be adequately decoupled.
 2. ON Semiconductor recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
 3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
 4. The parallel interface output pads can be left unconnected if the serial output interface is used.
 5. ON Semiconductor recommends that 0.1μF and 10μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0135AT demo headboard schematics for circuit recommendations.
 6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.
 7. Although 4 serial lanes are shown, the AR0135AT supports only 2 or 3 lane HiSPi.



AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor Configuration and Pinout

Figure 4: Typical Configuration: Parallel Pixel Data Interface

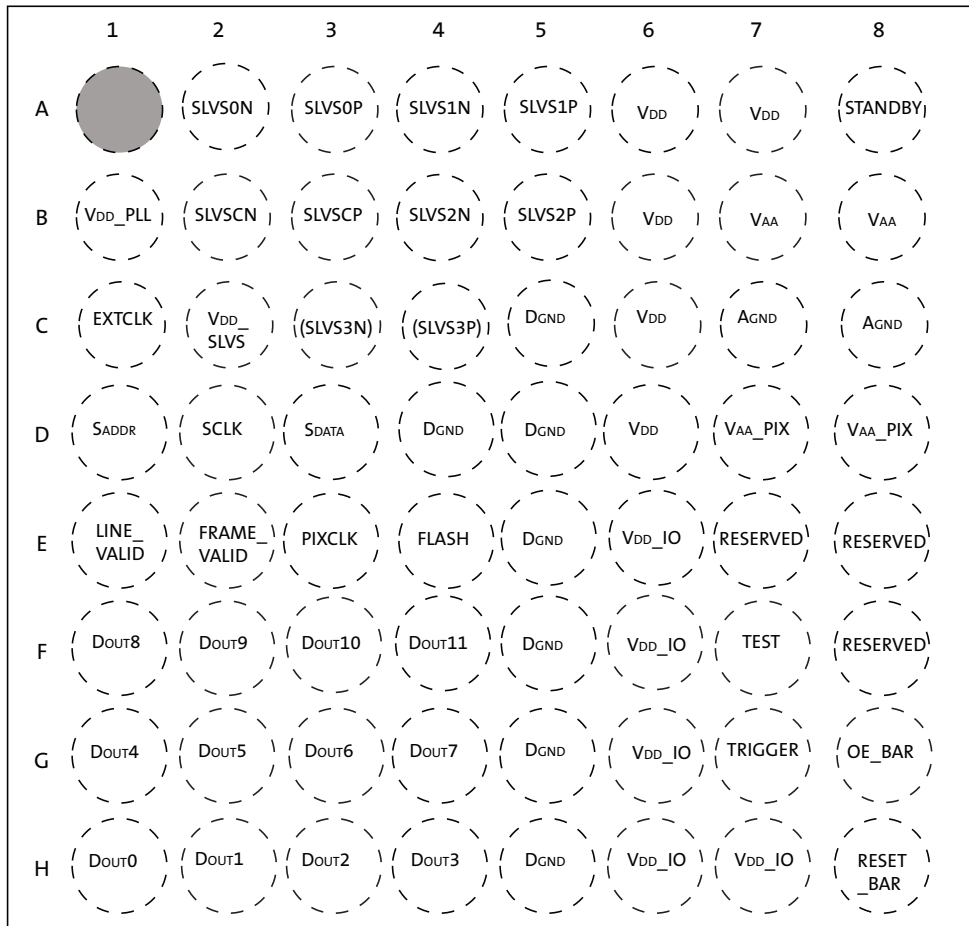


- Notes:
1. All power supplies must be adequately decoupled.
 2. ON Semiconductor recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
 3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
 4. The serial interface output pads can be left unconnected if the parallel output interface is used.
 5. ON Semiconductor recommends that 0.1μF and 10μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0135AT demo headboard schematics for circuit recommendations.
 6. ON Semiconductor recommends that analog power planes be placed in a manner such that coupling with the digital power planes is minimized.



AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor Configuration and Pinout

Figure 5: 9x9mm 63-Ball iBGA Package



Top View
(Ball Down)

AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor
Configuration and Pinout

Table 3: Pin Descriptions - 63-Ball iBGA Package

Name	iBGA Pin	Type	Description
SLVS0_N	A2	Output	HiSPi serial data, lane 0, differential N.
SLVS0_P	A3	Output	HiSPi serial data, lane 0, differential P.
SLVS1_N	A4	Output	HiSPi serial data, lane 1, differential N.
SLVS1_P	A5	Output	HiSPi serial data, lane 1, differential P.
STANDBY	A8	Input	Standby-mode enable pin (active HIGH).
VDD_PLL	B1	Power	PLL power.
SLVSC_N	B2	Output	HiSPi serial DDR clock differential N.
SLVSC_P	B3	Output	HiSPi serial DDR clock differential P.
SLVS2_N	B4	Output	HiSPi serial data, lane 2, differential N.
SLVS2_P	B5	Output	HiSPi serial data, lane 2, differential P.
VAA	B7, B8	Power	Analog power.
EXTCLK	C1	Input	External input clock.
VDD_SLVS	C2	Power	HiSPi power. (May leave unconnected if parallel interface is used)
SLVS3_N	C3	Output	(Unsupported) HiSPi serial data, lane 3, differential N.
SLVS3_P	C4	Output	(Unsupported) HiSPi serial data, lane 3, differential P.
DGND	C5, D4, D5, E5, F5, G5, H5	Power	Digital GND.
VDD	A6, A7, B6, C6, D6	Power	Digital power.
AGND	C7, C8	Power	Analog GND.
SADDR	D1	Input	Two-Wire Serial address select.
SCLK	D2	Input	Two-Wire Serial clock input.
SDATA	D3	I/O	Two-Wire Serial data I/O.
VAA_PIX	D7, D8	Power	Pixel power.
LINE_VALID	E1	Output	Asserted when DOUT line data is valid.
FRAME_VALID	E2	Output	Asserted when DOUT frame data is valid.
PIXCLK	E3	Output	Pixel clock out. DOUT is valid on rising edge of this clock.
FLASH	E4	Output	Control signal to drive external light sources.
VDD_IO	E6, F6, G6, H6, H7	Power	I/O supply power.
DOUT8	F1	Output	Parallel pixel data output.
DOUT9	F2	Output	Parallel pixel data output.
DOUT10	F3	Output	Parallel pixel data output.
DOUT11	F4	Output	Parallel pixel data output (MSB)
TEST	F7	Input	Manufacturing test enable pin (connect to DGND).
DOUT4	G1	Output	Parallel pixel data output.
DOUT5	G2	Output	Parallel pixel data output.
DOUT6	G3	Output	Parallel pixel data output.
DOUT7	G4	Output	Parallel pixel data output.
TRIGGER	G7	Input	Exposure synchronization input. (Connect to DGND if HiSPi interface is used)
OE_BAR	G8	Input	Output enable (active LOW).
DOUT0	H1	Output	Parallel pixel data output (LSB)
DOUT1	H2	Output	Parallel pixel data output.
DOUT2	H3	Output	Parallel pixel data output.
DOUT3	H4	Output	Parallel pixel data output.
RESET_BAR	H8	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
Reserved	E7, E8, F8	n/a	Reserved (do not connect).



Two-Wire Serial Register Interface

The two-wire serial interface bus enables read/write access to control and status registers within the AR0135AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the AR0135AT uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the AR0135AT are 0x20 (write address) and 0x21 (read address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the SADDR input.



An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

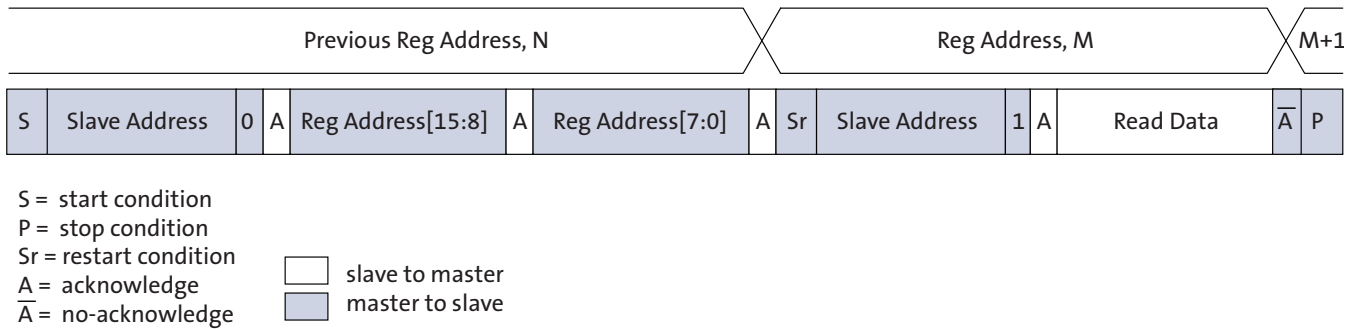
If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.



Single READ from Random Location

This sequence (Figure 6 on page 14) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 6 shows how the internal register address maintained by the AR0135AT is loaded and incremented as the sequence proceeds.

Figure 6: Single READ from Random Location



Single READ from Current Location

This sequence (Figure 7) performs a read using the current value of the AR0135AT internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

Figure 7: Single READ from Current Location

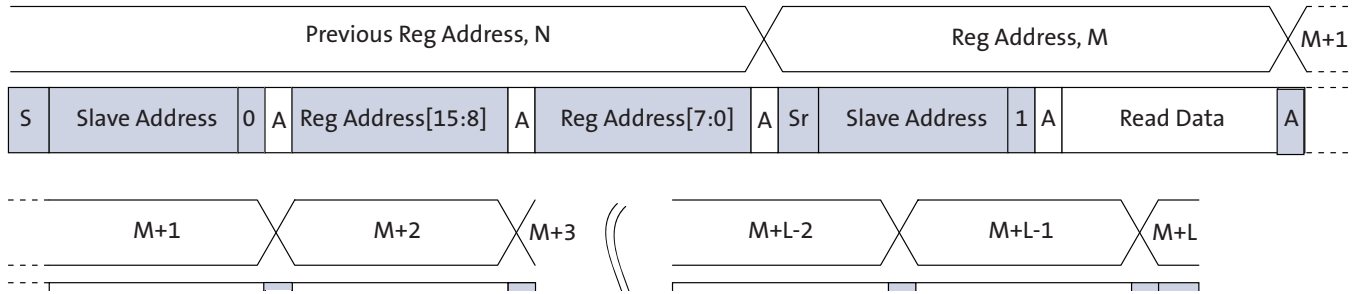




Sequential READ, Start from Random Location

This sequence (Figure 8) starts in the same way as the single READ from random location (Figure 6). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

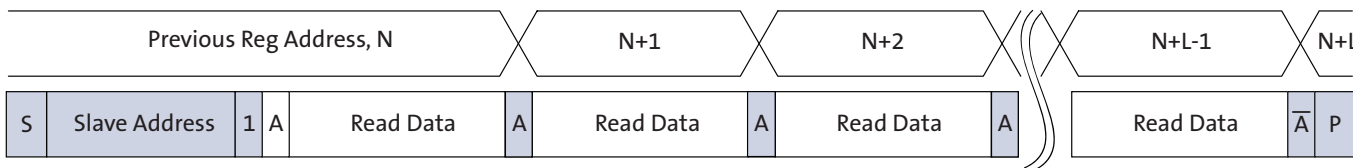
Figure 8: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 9) starts in the same way as the single READ from current location (Figure 7 on page 14). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

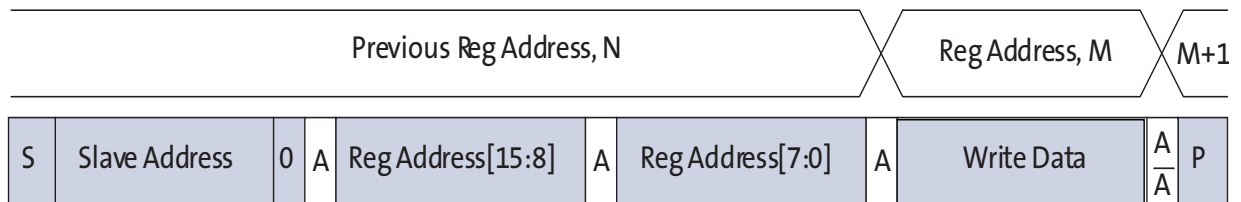
Figure 9: Sequential READ, Start from Current Location



Single WRITE to Random Location

This sequence (Figure 10) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

Figure 10: Single WRITE to Random Location

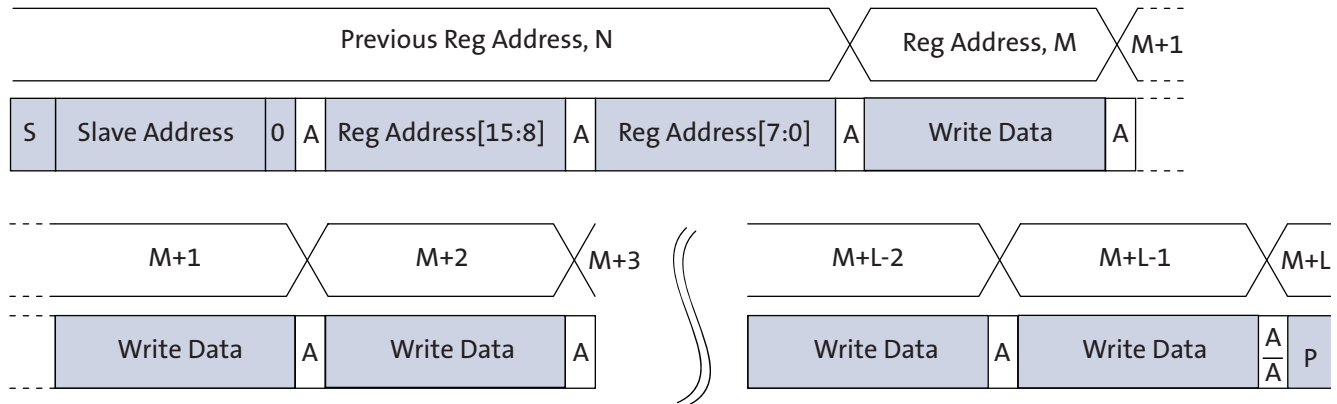




Sequential WRITE, Start at Random Location

This sequence (Figure 11) starts in the same way as the single WRITE to random location (Figure 10). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITES until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 11: Sequential WRITE, Start at Random Location





Electrical Specifications

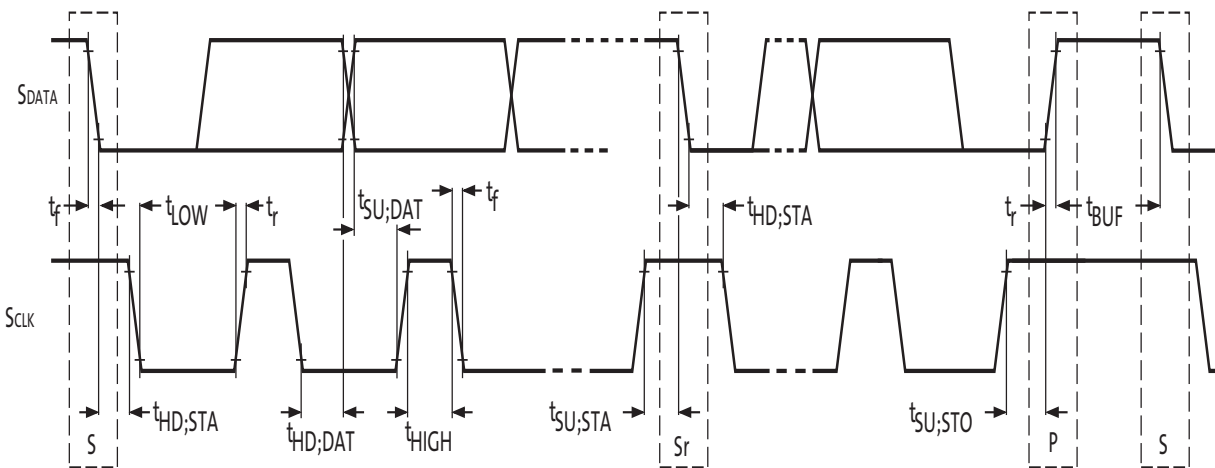
Unless otherwise stated, the following specifications apply to the following conditions:

$V_{DD} = 1.8V - 0.10/+0.15$; $V_{DD_IO} = V_{DD_PLL} = V_{AA} = V_{AA_PIX} = 2.8V \pm 0.3V$;
 $V_{DD_SLVS} = 0.4V - 0.1/+0.2$; $T_A = -30^{\circ}C$ to $+70^{\circ}C$; output load = 10pF;
 PIXCLK frequency = 74.25 MHz; HiSPi off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 12 and Table 4.

Figure 12: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Table 4: Two-Wire Serial Bus Characteristics

$f_{EXTCLK} = 27$ MHz; $V_{DD} = 1.8V$; $V_{DD_IO} = 2.8V$; $V_{AA} = 2.8V$; $V_{AA_PIX} = 2.8V$;
 $V_{DD_PLL} = 2.8V$; $V_{DD_DAC} = 2.8V$; $T_A = 25^{\circ}C$

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	f_{SCLK}	0	100	0	400	KHz
Hold time (repeated) START condition.						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	μS
LOW period of the SCLK clock	t_{LOW}	4.7	-	1.3	-	μS
HIGH period of the SCLK clock	t_{HIGH}	4.0	-	0.6	-	μS
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	μS
Data hold time:	$t_{HD;DAT}$	0^4	3.45^5	0^6	0.9^5	μS
Data set-up time	$t_{SU;DAT}$	250	-	100^6	-	nS
Rise time of both SDATA and SCLK signals	t_r	-	1000	$20 + 0.1Cb^7$	300	nS
Fall time of both SDATA and SCLK signals	t_f	-	300	$20 + 0.1Cb^7$	300	nS
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	μS


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 Electrical Specifications

Table 4: Two-Wire Serial Bus Characteristics
 $f_{EXTCLK} = 27 \text{ MHz}; V_{DD} = 1.8\text{V}; V_{DD_IO} = 2.8\text{V}; V_{AA} = 2.8\text{V}; V_{AA_PIX} = 2.8\text{V};$
 $V_{DD_PLL} = 2.8\text{V}; V_{DD_DAC} = 2.8\text{V}; T_A = 25^\circ\text{C}$

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min	Max	Min	Max	
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	μs
Capacitive load for each bus line	C_b	-	400	-	400	pF
Serial interface input pin capacitance	C_{IN_SI}	-	3.3	-	3.3	pF
SDATA max load capacitance	C_{LOAD_SD}	-	30	-	30	pF
SDATA pull-up resistor	RSD	1.5	4.7	1.5	4.7	$\text{K}\Omega$

- Notes:
1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
 2. Two-wire control is I²C-compatible.
 3. All values referred to $V_{IHmin} = 0.9 V_{DD}$ and $V_{ILmax} = 0.1 V_{DD}$ levels. Sensor EXCLK = 27 MHz.
 4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
 5. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCLK signal.
 6. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} = 250 \text{ ns}$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line $t_r \text{ max} + t_{SU;DAT} = 1000 + 250 = 1250 \text{ ns}$ (according to the Standard-mode I²C-bus specification) before the SCLK line is released.
 7. C_b = total capacitance of one bus line in pF.



I/O Timing

By default, the AR0135AT launches pixel data, FV and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV and LV using the rising edge of PIXCLK. The launch edge of PIXCLK can be configured in register R0x3028. See Figure 13 and Table 5 for I/O timing (AC) characteristics.

Figure 13: I/O Timing Diagram

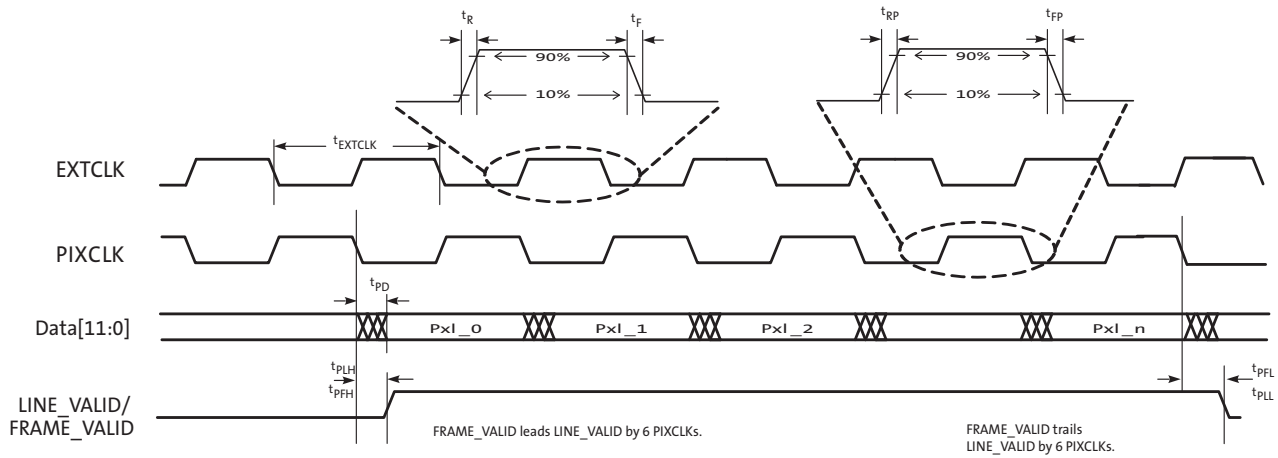


Table 5: I/O Timing Characteristics, Parallel Output (1.8V VDD_IO)¹

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_EXTCLK	Input clock frequency		6		50	MHz
t_EXTCLK	Input clock period		20		166	ns
t_R	Input clock rise time	PLL enabled		3		ns
t_F	Input clock fall time	PLL enabled		3		ns
t_JITTER	Input clock jitter				600	ns
t_cp	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL disabled, PIXCLK slew rate = 4	5.7		14.3	ns
t_RP	PIXCLK rise time	PCLK slew rate = 6	1.3		4.0	ns
t_FP	PIXCLK fall time	PCLK slew rate = 6	1.3		3.9	ns
	PIXCLK duty cycle		40	50	60	%
f_PIXCLK	PIXCLK frequency	PIXCLK slew rate = 6, Data slew rate = 7	6		74.25	MHz
t_PD	PIXCLK to data valid	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_PFH	PIXCLK to FV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_PLH	PIXCLK to LV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-3		1.5	ns
t_PFL	PIXCLK to FV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t_PLL	PIXCLK to LV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-3		1.5	ns
CIN	Input pin capacitance			2.5		pf



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- Notes: 1. Minimum and maximum values are taken at 70°C, 1.7V and -30°C, 1.95V. All values are taken at the 50% transition point. The loading used is 10 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 6: I/O Timing Characteristics, Parallel Output (2.8V V_{DD_IO})¹

Symbol	Definition	Condition	Min	Typ	Max	Unit
f _{EXTCLK}	Input clock frequency		6		50	MHz
t _{EXTCLK}	Input clock period		20		166	ns
t _R	Input clock rise time	PLL enabled		3		ns
t _F	Input clock fall time	PLL enabled		3		ns
t _{JITTER}	Input clock jitter				600	ns
t _{cp}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL disabled, PIXCLK slew rate = 4	5.3		13.4	ns
t _{RP}	PIXCLK rise time	PCLK slew rate = 6	1.3		4.0	ns
t _{FP}	PIXCLK fall time	PCLK slew rate = 6	1.3		3.9	ns
	PIXCLK duty cycle		40	50	60	%
f _{PIXCLK}	PIXCLK frequency	PIXCLK slew rate = 6, Data slew rate = 7	6		74.25	MHz
t _{PD}	PIXCLK to data valid	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t _{PFH}	PIXCLK to FV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t _{PLH}	PIXCLK to LV HIGH	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t _{PFL}	PIXCLK to FV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
t _{PLL}	PIXCLK to LV LOW	PIXCLK slew rate = 6, Data slew rate = 7	-2.5		2	ns
C _{IN}	Input pin capacitance			2.5		pf

- Notes: 1. Minimum and maximum values are taken at 70°C, 2.5V and -30°C, 3.1V. All values are taken at the 50% transition point. The loading used is 10 pF.
2. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.

Table 7: I/O Rise Slew Rate (2.8V V_{DD_IO})¹

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.50	2.50	3.90	V/ns
6	Default	0.98	1.62	2.52	V/ns
5	Default	0.71	1.12	1.79	V/ns
4	Default	0.52	0.82	1.26	V/ns
3	Default	0.37	0.58	0.88	V/ns
2	Default	0.26	0.40	0.61	V/ns
1	Default	0.17	0.27	0.40	V/ns
0	Default	0.10	0.16	0.23	V/ns

Note: 1. Minimum and maximum values are taken at 70°C, 2.5V and -30°C, 3.1V.
The loading used is 10 pF.

Table 8: I/O Fall Slew Rate (2.8V V_{DD_IO})¹

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.40	2.30	3.50	V/ns
6	Default	0.97	1.61	2.48	V/ns
5	Default	0.73	1.21	1.86	V/ns
4	Default	0.54	0.88	1.36	V/ns
3	Default	0.39	0.63	0.88	V/ns
2	Default	0.27	0.43	0.66	V/ns
1	Default	0.18	0.29	0.44	V/ns
0	Default	0.11	0.17	0.25	V/ns

Note: 1. Minimum and maximum values are taken at 70°C, 2.5V and -30°C, 3.1V.
The loading used is 10 pF.

**Table 9: I/O Rise Slew Rate (1.8V VDD_IO)¹**

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.57	0.91	1.55	V/ns
6	Default	0.39	0.61	1.02	V/ns
5	Default	0.29	0.46	0.75	V/ns
4	Default	0.22	0.34	0.54	V/ns
3	Default	0.16	0.24	0.39	V/ns
2	Default	0.12	0.17	0.27	V/ns
1	Default	0.08	0.11	0.18	V/ns
0	Default	0.05	0.07	0.10	V/ns

Note: 1. Minimum and maximum values are taken at 70°C, 1.7V and -30°C, 1.95V.
The loading used is 10 pF.

Table 10: I/O Fall Slew Rate (1.8V VDD_IO)¹

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.57	0.92	1.55	V/ns
6	Default	0.40	0.64	1.08	V/ns
5	Default	0.31	0.50	0.82	V/ns
4	Default	0.24	0.38	0.61	V/ns
3	Default	0.18	0.27	0.44	V/ns
2	Default	0.13	0.19	0.31	V/ns
1	Default	0.09	0.13	0.20	V/ns
0	Default	0.05	0.08	0.12	V/ns

Notes: 1. Minimum and maximum values are taken at 70°C, 1.7V and -30°C, 1.95V.
The loading used is 10 pF.



DC Electrical Characteristics

The DC electrical characteristics are shown in Table 11, Table 12, Table 13, and Table 14.

Table 11: DC Electrical Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
VDD	Core digital voltage		1.7	1.8	1.95	V
VDD_IO	I/O digital voltage		1.7/2.5	1.8/2.8	1.9/3.1	V
VAA	Analog voltage		2.5	2.8	3.1	V
VAA_PIX	Pixel supply voltage		2.5	2.8	3.1	V
VDD_PLL	PLL supply voltage		2.5	2.8	3.1	V
VDD_SLVS	HiSPi supply voltage		0.3	0.4	0.6	V
VIH	Input HIGH voltage		VDD_IO * 0.7	–	–	V
VIL	Input LOW voltage		–	–	VDD_IO * 0.3	V
IIN	Input leakage current	No pull-up resistor; VIN = VDD_IO or DGND	20	–	–	μA
VOH	Output HIGH voltage		VDD_IO – 0.3	–	–	V
VOL	Output LOW voltage	VDD_IO = 2.8V	–	–	0.4	V
IOH	Output HIGH current	At specified VOH	–22	–	–	mA
IOL	Output LOW current	At specified VOL	–	–	22	mA

Caution Stresses greater than those listed in Table 12 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Table 12: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Symbol
VSUPPLY	Power supply voltage (all supplies)	–0.3	4.5	V	VSUPPLY
ISUPPLY	Total power supply current	–	200	mA	ISUPPLY
IGND	Total ground current	–	200	mA	IGND
VIN	DC input voltage	–0.3	VDD_IO + 0.3	V	VIN
VOUT	DC output voltage	–0.3	VDD_IO + 0.3	V	VOUT
TSTG ¹	Storage temperature	–40	+125	°C	TSTG ¹

Note: 1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 13: Operating Current Consumption for Parallel Output

VAA = VAA_PIX = VDD_IO = VDD_PLL = 2.8V; VDD = 1.8V; PLL Enabled and PIXCLK = 74.25 MHz; TA = 25°C; CLOAD = 10pF

	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	Parallel, Streaming, Full resolution 54 fps	IDD1		46	60	mA
I/O digital operating current	Parallel, Streaming, Full resolution 54 fps	IDD_IO		52	–	mA
Analog operating current	Parallel, Streaming, Full resolution 54 fps	IAA		46	55	mA
Pixel supply current	Parallel, Streaming, Full resolution 54 fps	IAA_PIX		7	9	mA
PLL supply current	Parallel, Streaming, Full resolution 54 fps	IDD_PLL		8	10	mA

**Table 14: Standby Current Consumption**Analog - VAA + VAA_PIX + VDD_PLL; Digital - VDD + VDD_IO; T_A = 25°C

Definition	Condition	Min	Typ	Max	Unit
Hard standby (clock off, driven low)	Analog, 2.8V	–	3	15	μA
	Digital, 1.8V	–	25	125	μA
Hard standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V	–	12	25	μA
	Digital, 1.8V	–	1.1	1.7	mA
Soft standby (clock off, driven low)	Analog, 2.8V	–	3	15	μA
	Digital, 1.8V	–	25	125	μA
Soft standby (clock on, EXTCLK = 20 MHz)	Analog, 2.8V	–	12	25	μA
	Digital, 1.8V	–	1.1	1.7	mA

HiSPi Electrical Specifications

The ON Semiconductor AR0135AT sensor supports SLVS mode only, and does not have a DLL for timing adjustments. Refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The VDD_SLVS supply in this data sheet corresponds to VDD_TX in the HiSPi Physical Layer Specification. Similarly, VDD is equivalent to VDD_HiSPi as referenced in the specification. The HiSPi transmitter electrical specifications are listed at 700 MHz.

Table 15: Input Voltage and Current (HiSPi Power Supply 0.4 V)

Measurement Conditions: Max Freq 700 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Supply current (PWR _{HiSPi}) (driving 100Ω load)	I _{DD_SLVS}	–	10	15	mA
HiSPi common mode voltage (driving 100Ω load)	V _{CM}	V _{DD_SLVS} x 0.45	V _{DD_SLVS} /2	V _{DD_SLVS} x 0.55	V
HiSPi differential output voltage (driving 100Ω load)	V _{OD}	V _{DD_SLVS} x 0.36	V _{DD_SLVS} /2	V _{DD_SLVS} x 0.64	V
Change in V _{CM} between logic 1 and 0	ΔV _{CM}			25	mV
Change in V _{OD} between logic 1 and 0	V _{OD}			25	mV
V _{OD} noise margin	NM	–		30	%
Difference in V _{CM} between any two channels	ΔV _{CM}			50	mV
Difference in V _{OD} between any two channels	ΔV _{OD}			100	mV
Common-mode AC voltage (pk) without V _{CM} cap termination	ΔV _{CM_ac}			50	mV
Common-mode AC voltage (pk) with V _{CM} cap termination	ΔV _{CM_ac}			30	mV
Max overshoot peak V _{OD}	V _{OD_ac}			1.3 x V _{OD}	V
Max overshoot V _{diff} pk-pk	V _{diff_pkpk}			2.6 x V _{OD}	V
Eye Height	V _{eye}	1.4 x V _{OD}			
Single-ended output impedance	R _o	35	50	70	Ω
Output impedance mismatch	ΔR _o			20	%



Figure 14: Differential Output Voltage for Clock or Data Pairs

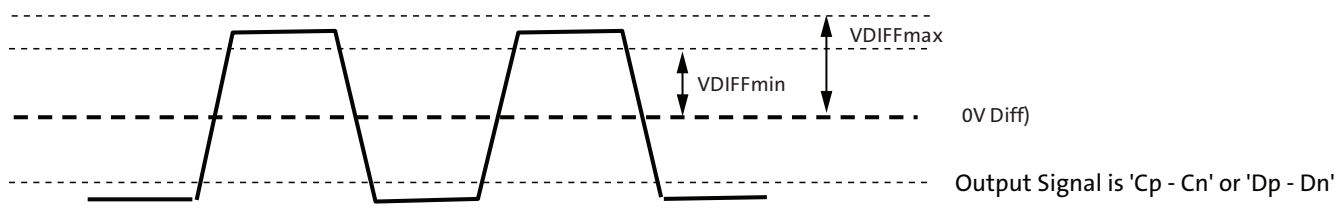


Table 16: Rise and Fall Times

Measurement Conditions: HiSPi Power Supply 0.4V, Max Freq 700 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate	1/UI	280	–	700	Mb/s
Max setup time from transmitter	TxPRE	0.3	–	–	UI ¹
Max hold time from transmitter	TxPost	0.3	–	–	UI
Rise time (20% - 80%)	RISE	–	0.25UI	–	
Fall time (20% - 80%)	FALL	150ps	0.25 UI	–	
Clock duty	PLL_DUTY	45	50	55	%
Bitrate Period	t _{pw}	1.43		3.57	ns ¹
Eye Width	t _{eye}	0.3			UI ^{1, 2}
Data Total jitter (pk pk)@1e-9	t _{totaljit}			0.2	UI ^{1, 2}
Clock Period Jitter (RMS)	t _{ckjit}			50	ps ²
Clock cycle to cycle jitter (RMS)	t _{cyj}			100	ps ²
Clock to Data Skew	t _{chskew}	-0.1		0.1	UI ^{1, 2}
PHY-to-PHY Skew	t _{PHYSkew}			2.1	UI ^{1, 5}
Mean differential skew	t _{DIFFSKEW}	-100		100	ps ⁶

- Notes:
1. One UI is defined as the normalized mean time between one edge and the following edge of the clock.
 2. Taken from 0V crossing point.
 3. Also defined with a maximum loading capacitance of 10pF on any pin. The loading capacitance may also need to be less for higher bitrates so the rise and fall times do not exceed the maximum 0.3UI.
 4. The absolute mean skew between the Clock lane and any Data Lane in the same PHY between any edges.
 5. The absolute mean skew between any Clock in one PHY and any Data lane in any other PHY between any edges.
 6. Differential skew is defined as the skew between complementary outputs. It is measured as the absolute time between the two complementary edges at mean V_{CM} point.



Figure 15: Eye Diagram for Clock and Data Signals

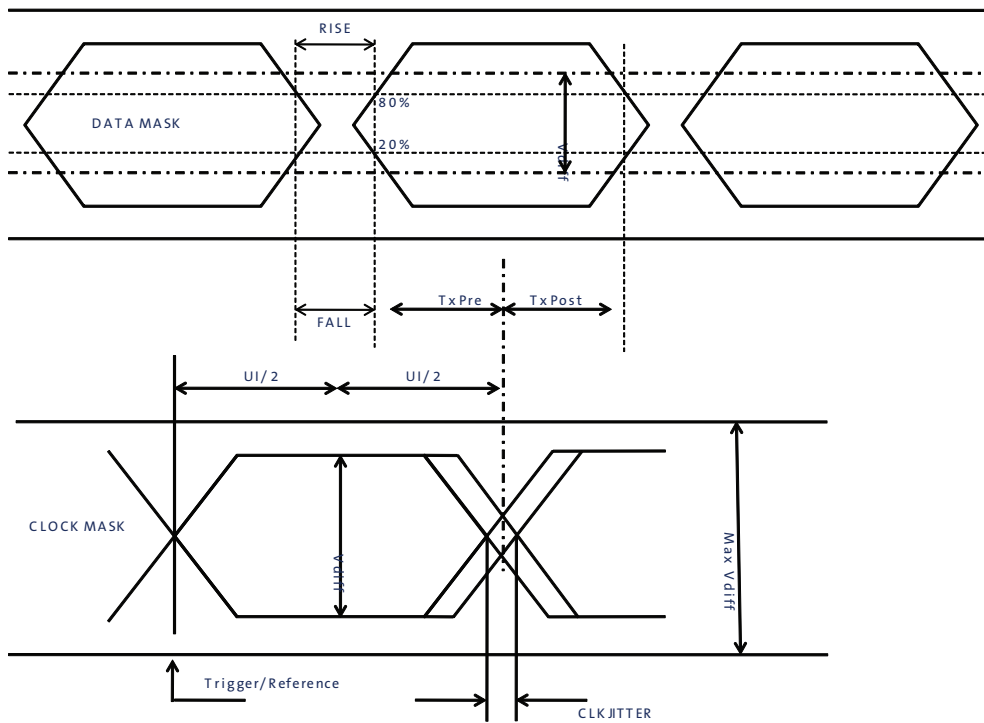
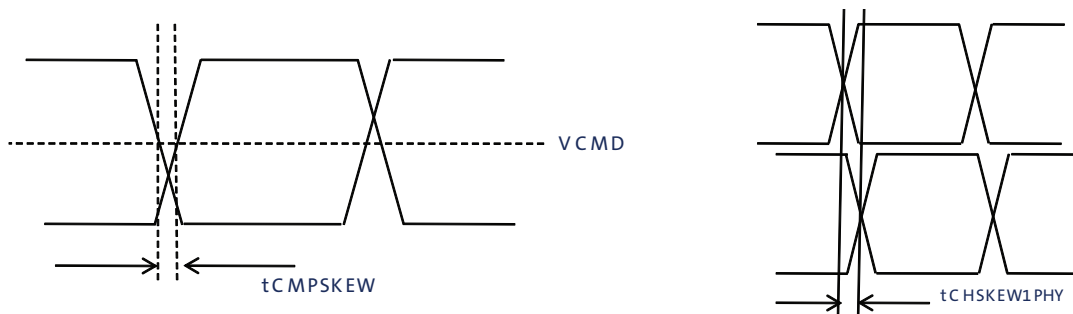


Figure 16: Skew Within the PHY and Output Channels





AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor
Power-On Reset and Standby Timing

Power-On Reset and Standby Timing

Power-Up Sequence

The recommended power-up sequence for the AR0135AT is shown in Figure 17. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL power supply.
2. After 0–10 μ s, turn on VAA and VAA_PIX power supply.
3. After 0–10 μ s, turn on VDD_IO power supply.
4. After the last power supply is stable, enable EXTCLK.
5. If RESET_BAR is in a LOW state, hold RESET_BAR LOW for at least 1 ms.
If RESET_BAR is in a HIGH state, assert RESET_BAR for at least 1 ms.
6. Wait 160000 EXTCLKs (for internal initialization into software standby).
7. Configure PLL, output, and image settings to desired values.
8. Wait 1 ms for the PLL to lock.
9. Set streaming mode (R0x301A[2] = 1).

Figure 17: Power Up

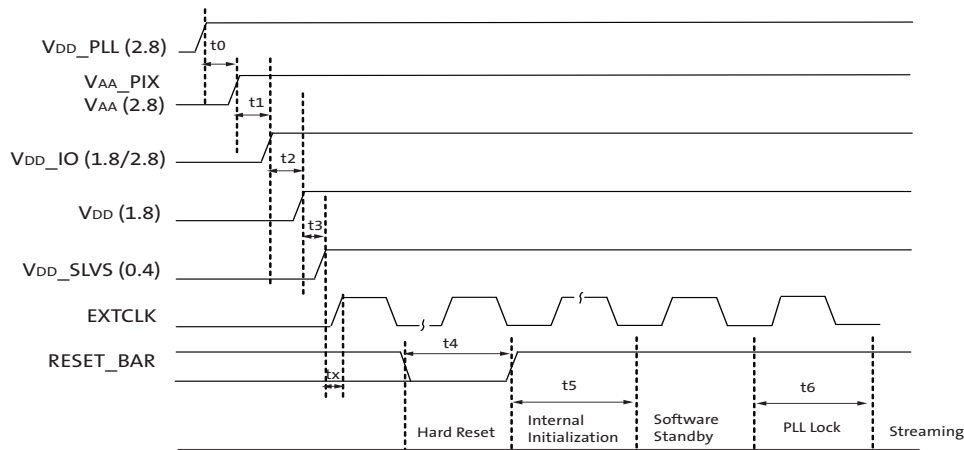


Table 17: Power-Up Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX	t0	0	10	–	μ s
VAA/VAA_PIX to VDD_IO	t1	0	10	–	μ s
VDD_IO to VDD	t2	0	10	–	μ s
VDD to VDD_SLVS	t3	0	10	–	μ s
Xtal settle time	tx	–	30 ¹	–	ms
Hard Reset	t4	1 ²	–	–	ms
Internal Initialization	t5	160000	–	–	EXTCLKs
PLL Lock Time	t6	1	–	–	ms

- Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
 2. Hard reset time is the minimum time required after power rails are settled. In a circuit where hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
 3. It is critical that VDD_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD_PLL is powered after



AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor
Power-On Reset and Standby Timing

other supplies then the sensor may have functionality issues and will experience high current draw on this supply.

Power-Down Sequence

The recommended power-down sequence for the AR0135AT is shown in Figure 18. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301A[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off VDD_SLVS.
4. Turn off VDD.
5. Turn off VDD_IO
6. Turn off VAA/VAA_PIX.
7. Turn off VDD_PLL.

Figure 18: Power Down

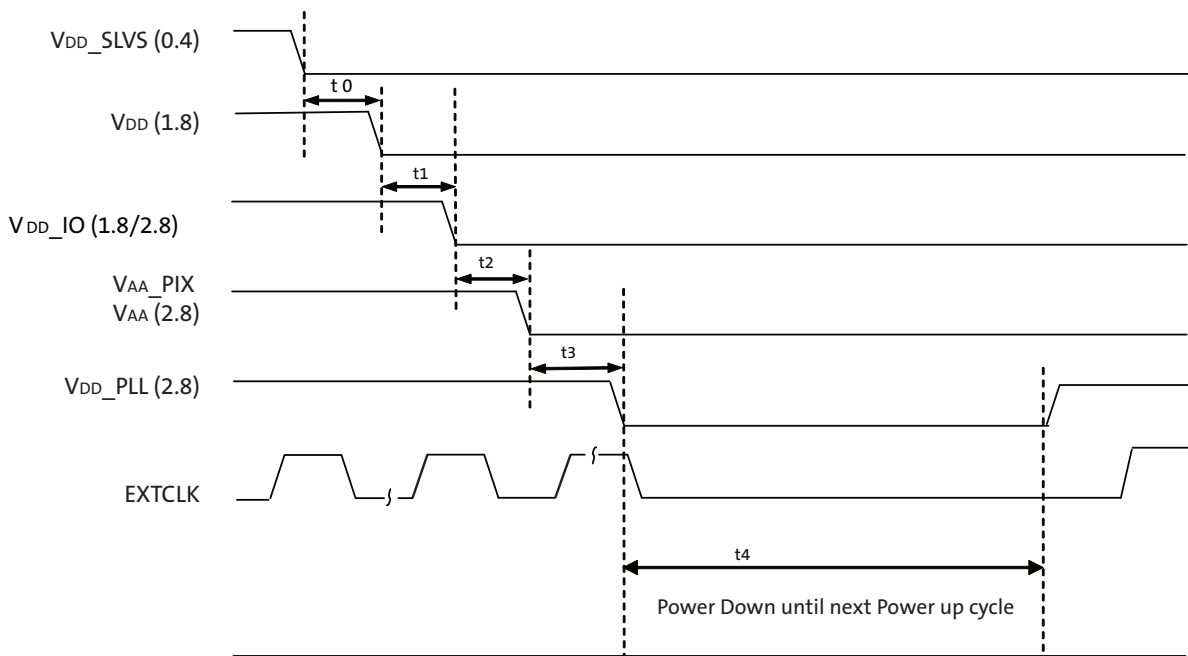


Table 18: Power-Down Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_SLVS to VDD	t0	0	–	–	μs
VDD to VDD_IO	t1	0	–	–	μs
VDD_IO to VAA/VAA_PIX	t2	0	–	–	μs
VAA/VAA_PIX to VDD_PLL	t3	0	–	–	μs
PwrDn until Next PwrUp Time	t4	100	–	–	ms

Note: t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.



Standby Sequence

Figures 19 and 20 show timing diagrams for entering and exiting standby. Delays are shown indicating the last valid register write prior to entering standby as well as the first valid write upon exiting standby. Also shown is timing if the EXTCLK is to be disabled during standby.

Figure 19: Enter Standby Timing

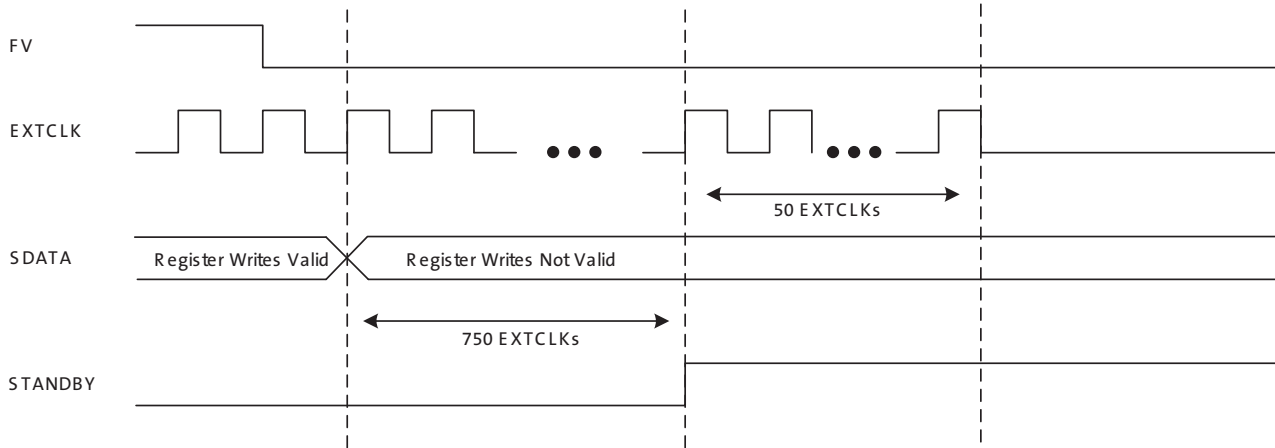


Figure 20: Exit Standby Timing

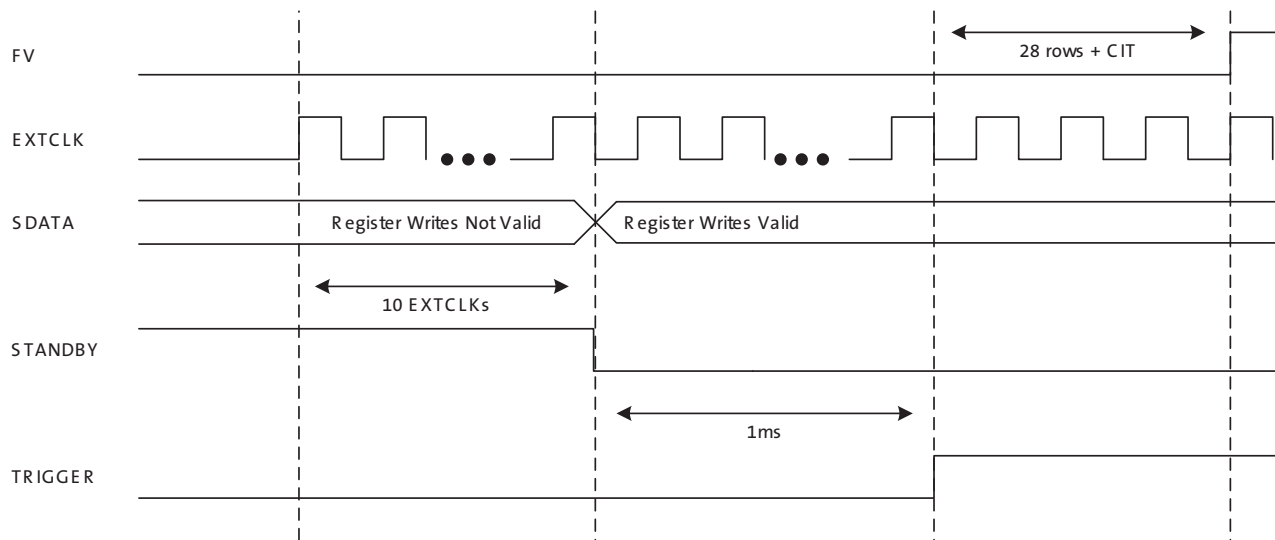
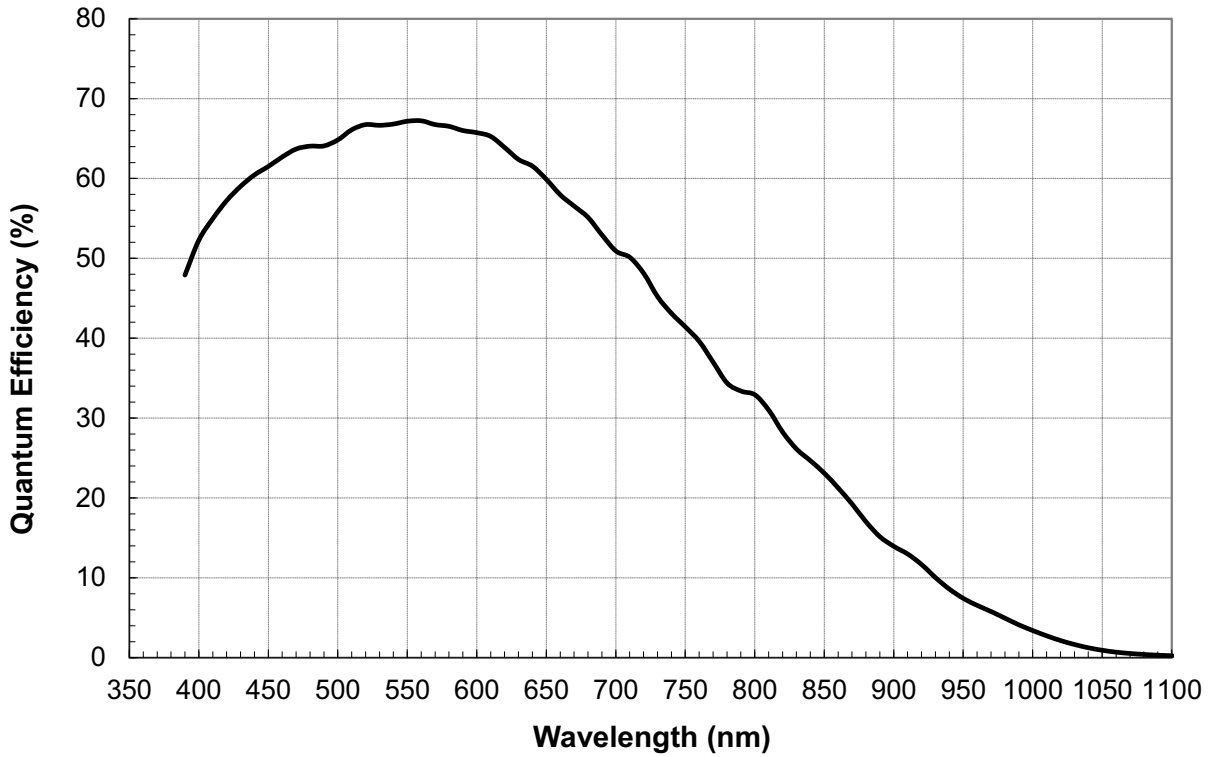




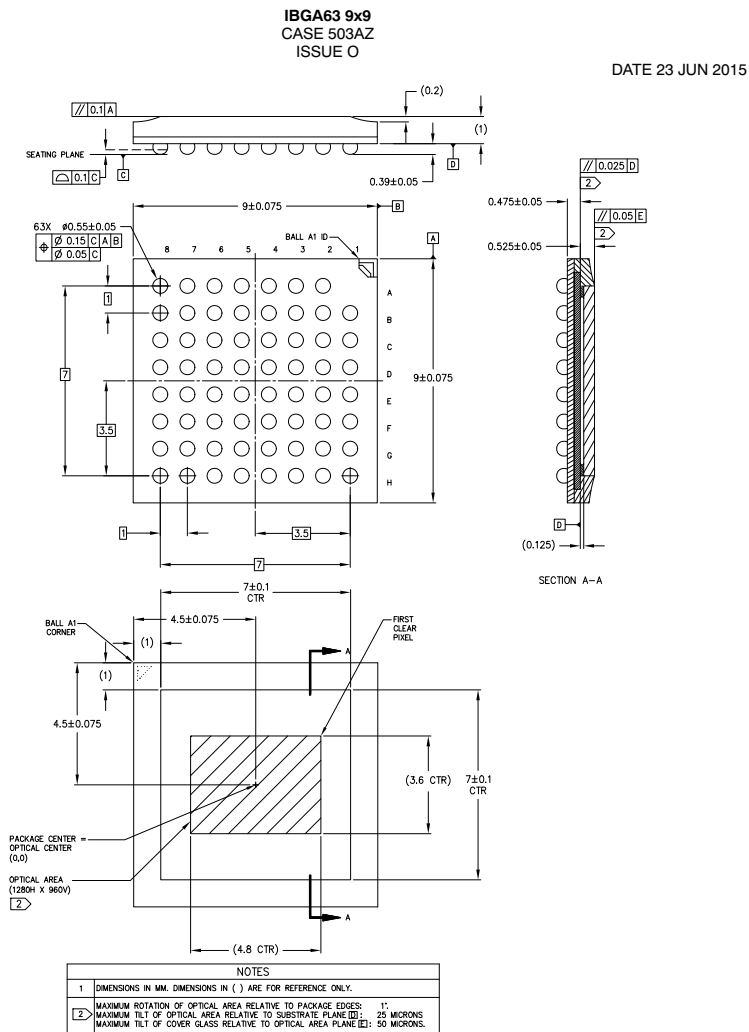
Figure 21: Quantum Efficiency – Monochrome Sensor (Typical)





Package Dimensions

Figure 22: 63-Ball iBGA Package Outline Drawing



- Notes:
- Lid material: Borosilicate glass 0.4 ± 0.04 thickness. Refractive index at 20C = 1.5255 @ 546 nm and 1.5231 @ 588 nm. Double side AR Coating: 530-570nm R < 1%; 420-700nm R < 2%.
 - Solder ball material: SAC305 (95% Sn, 3% Ag, 0.5% Cu). Dimensions apply to solder balls post reflow. Pre-flow ball is 0.5 on a $\varnothing 0.4$ SMD ball pad.



AR0135AT 1/3-Inch 1.2Mp CMOS Digital Image Sensor

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